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front surface. The rear surface of the second semiconductor chip is juxtaposed with the front surface of the first semiconductor chip. The assembly includes a first backing element having electrically conductive first terminals. The first backing element is juxtaposed with the rear surface of the first semiconductor chip so that at least some of the terminals overlie the rear surface of the first semiconductor chip. At least some of the contacts on the first and the second semiconductor chips are electrically connected to at least some of the terminals. The assembly includes a substrate having contact pads thereon. The first terminals are connected to the contact pads of the substrate. The substrate is adapted to connect the assembly with other elements of a circuit. At least some of the first terminals overlie the rear surface of the first semiconductor chip.

IN THE CLAIMS:

Cancel claim 1.

Insert new claims 2-62 as follows:

A6

1 x. A semiconductor chip assembly, comprising:

a) a first semiconductor chip having a front surface, a rear surface and contacts on said front surface;

b) a second semiconductor chip having a front surface, a rear surface and contacts on said front surface, said rear surface of said second semiconductor chip being juxtaposed with said front surface of said first semiconductor chip;

c) a first backing element having electrically conductive first terminals, said first backing element being juxtaposed with said rear surface of said first semiconductor chip so that at least some of said terminals overlie said rear surface of said first semiconductor chip, at least some of said contacts on said first and said second semiconductor

A6 Cont'd.

chips being electrically connected to at least some of said terminals; and

d) a substrate having contact pads thereon, said first terminals being connected to said contact pads of said substrate, said substrate being adapted to connect the assembly with other elements of a circuit, at least some of said first terminals overlying said rear surface of said first semiconductor chip.

2 8. The assembly as claimed in claim 1 wherein said first terminals are movable with respect to said first chip to compensate for differential thermal expansion of said first chip and said substrate.

3 9. The assembly as claimed in claim 2 wherein said first semiconductor chip and said substrate have different coefficients of thermal expansion.

4 10. The assembly as claimed in claim 1 wherein said first backing element has electrically conductive lead portions thereon connected to said terminals and wherein said terminals are electrically connected to at least some of said contact on said first and second semiconductor chips through said lead portions.

5 11. The assembly as claimed in claim 4 further comprising first bonding wires extending between at least some of said contacts of said first semiconductor chip and said lead portions so that said terminals of said first backing element are electrically connected to at least some of the contacts on said first semiconductor chip through said

lead portions and said first bonding wires.

6 ~~7~~. The assembly as claimed in claim 5 ~~6~~, further comprising a dielectric encapsulant covering at least a portion of said first bonding wires.

7 ~~8~~. The assembly as claimed in claim 6 ~~7~~, wherein the encapsulant is compliant.

8 ~~9~~. The assembly as claimed in claim 1 ~~2~~, further comprising a dielectric encapsulant covering at least a portion of the electrical connections between the contacts on the chip and the terminals of said first backing element.

9 ~~10~~. The assembly as claimed in claim 8 ~~9~~, wherein the encapsulant is compliant.

10 ~~11~~. The assembly as claimed in claim 1 ~~2~~ wherein said contacts of said second semiconductor chip are electrically connected to said terminals on said first backing element through at least some of said contacts on said first semiconductor chip.

11 ~~12~~. The assembly as claimed in claim 1 ~~2~~ wherein at least some of said contacts on said first semiconductor chip are connected to at least some of said contacts on said second semiconductor chip.

12 ~~13~~. The assembly as claimed in claim 11 ~~12~~ further comprising a second backing element extending between said

first and second semiconductor chips, said second backing element having terminals thereon, at least some of said contacts on said second semiconductor chip being connected to at least some of said contacts on said first semiconductor chip through said terminals of said second backing element.

13
~~14~~. The assembly as claimed in any of claims 2 through 11 ~~12~~, further comprising a first compliant layer disposed between said backing element and said rear surface of said first semiconductor chip.

14 13
~~15~~. The assembly as claimed in claim ~~11~~, further comprising a second compliant layer disposed between said front surface of said first semiconductor chip and said rear surface of said second semiconductor chip.

15 13
~~16~~. The assembly as claimed in claim ~~14~~ wherein said first compliant layer incorporates an adhesive.

16 1
~~17~~. The assembly as claimed in any of claims ~~1~~ through 11 ~~12~~ wherein said terminals of said first backing element are engaged with said contact pads of said substrate.

17 1
~~18~~. The assembly as claimed in claim ~~1~~ wherein said terminals of said first backing element are bonded to contact pads of said substrate.

18 1
~~19~~. The assembly as claimed in claim ~~1~~, wherein said terminals of said backing element are solder-bonded to said contact pads of said substrate.

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19 1

~~20~~. The assembly as claimed in any of claims ~~1~~ through 11 ~~12~~, wherein said substrate is a circuit panel.

20 4

~~21~~. The assembly as claimed in any of claims ~~5~~ through 6 ~~7~~ wherein said first backing element has a bottom surface facing away from said rear surface of said first chip and has holes extending to said bottom surface, said terminals being disposed in alignment with said holes.

21 20

~~22~~. The assembly as claimed in claim ~~22~~ wherein said first backing element has a top surface facing toward said first chip and said lead portions and terminals are disposed at said top surface.

22 4

~~23~~. The assembly as claimed in any of claims ~~5~~ through 6 ~~7~~, wherein:

a) said first backing element has a top surface facing toward the chip and a bottom surface facing away from the chip; and

b) said lead portions and terminals disposed at said bottom surface of said first backing element.

23 22

~~24~~. The assembly as claimed in claim ~~23~~ further including a flexible dielectric material connected to and covering at least a portion of said bottom surface of said first backing element, wherein said flexible dielectric material has apertures therein, said terminals of said first

backing element being connected to said contact pads through said apertures.

24
~~25~~. The assembly as claimed any of claims 2 through 11 ~~12~~, wherein said first backing element is flexible to facilitate the movement of the terminals with respect to the chip.

25 24
~~26~~. The assembly as claimed in claim ~~25~~, wherein said first backing element includes a polymeric dielectric material.

26 25
~~27~~. The assembly as claimed in claim ~~26~~, wherein said first backing element includes a flexible sheet of a material selected from the group comprising polyimide, fluoropolymers, thermoplastic polymer and elastomer.

27 4
~~28~~. The assembly as claimed in any of claims ~~3~~ through 6 ~~7~~, wherein the first backing element is adapted to control the impedance of said lead portions .

28 27
~~29~~. The assembly as claimed in claim ~~28~~, wherein the first backing element includes an electrically conductive layer adapted to aid the electrical isolation of the terminals from the chip and to provide better control of impedance in said lead portions.

29 1
~~30~~. The assembly as claimed in any of claims ~~2~~ through 11 ~~12~~, wherein said terminals are movable in a direction parallel to said rear surface of said chip.

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30 1

~~31~~. The assembly as claimed in any of claims ~~1~~ through ~~12~~ wherein the terminals are movable in a direction perpendicular to said rear surface of said chip.

31 1

~~32~~. The assembly as claimed in any of claims ~~1~~ through ~~12~~, further comprising a third semiconductor chip having a front surface, a rear surface and contacts on said front surface, said rear surface of said third semiconductor chip being juxtaposed with said front surface of said second semiconductor chip.

33. A semiconductor chip assembly comprising:

(a) a first semiconductor chip having a front surface, a rear surface and contacts on said front surface;

(b) a substrate having contact pads thereon, said substrate extending beneath the rear surface of the first semiconductor chip so that said front surface of said first semiconductor chip faces upwardly away from said substrate, at least some of said contacts on said first semiconductor chip being electrically connected to said contact pads of said substrate, said substrate being adapted to connect the first semiconductor chip with other elements of a circuit; and

(c) a second semiconductor chip having front and rear surfaces and having contacts on said front surface, said second semiconductor chip overlying said front surface of said first semiconductor chip, at least some of said contacts on said second semiconductor chip being connected to at least some of said contacts on said first semiconductor chip, said second semiconductor chip being movable with

respect to said first semiconductor chip.

34. An assembly as claimed in claim 33 further comprising terminals connected to said contacts of said second semiconductor chip, at least some of said terminals overlying a surface of said second semiconductor chip, said terminals overlying said surface of said second semiconductor chip being movable with respect to said second semiconductor chip, said contacts of said second semiconductor chip being connected to said contacts of said first semiconductor chip through said terminals.

35. An assembly as claimed in claim 34 further comprising a dielectric element having said terminals thereon, said dielectric element having a central region disposed between said first and second semiconductor chips, at least some of said terminals being disposed in said central region.

36. An assembly as claimed in claim 33 wherein said rear surface of said second semiconductor chip faces downwardly toward said front surface of said first semiconductor chip, and wherein said central region of said dielectric element is disposed between said semiconductor chips.

37. An assembly as claimed in claim 35 wherein said front surface of said semiconductor chip faces downwardly toward said front surface of said first semiconductor chip, and wherein central region of said dielectric element overlies said front surface of said second

semiconductor chip.

36 33

38. An assembly as claimed in claim 35 further comprising a compliant layer disposed between said central region of said dielectric element and said second semiconductor chip.

37 34

39. An assembly as claimed in claim 36 further comprising a compliant layer disposed between said central region of said dielectric element and said second semiconductor chip.

38 35

40. An assembly as claimed in claim 37 further comprising a compliant layer disposed between said central region of said dielectric element and said second semiconductor chip.

41. An assembly as claimed in claim 33 further comprising terminals overlying said front surface of said first semiconductor chip, said terminals being movable with respect to said first semiconductor chip, said terminals being movable with respect to said first semiconductor chip, at least some of said contacts of said second semiconductor chip being connected to at least some of said contacts on said first semiconductor chip through said terminals.

40 39

42. An assembly as claimed in claim 41 further comprising a dielectric element overlying said first semiconductor chip, said dielectric element having said terminals thereon.

41 38
~~43~~. An assembly as claimed in claim ~~40~~ further comprising a compliant layer disposed between said dielectric element and said front surface of said first semiconductor chip.

42
~~41~~. An assembly as claimed in claim 35 or claim 36 or claim ~~37~~ 35 or claim ~~38~~ 36 or claim 39 or claim 40 or claim 42 or claim 43 wherein said dielectric element is flexible.

43 42
45. An assembly as claimed in claim ~~44~~ wherein said compliant layer has an elastic modulus lower than the elastic modulus of said dielectric element.

46. An assembly as claimed in claim 33 further comprising a compliant layer disposed between said semiconductor chips.

47. An assembly as claimed in claim 33 further comprising bonding wires, at least some of said contacts on said first semiconductor chip being electrically connected to contact pads on said substrate by said bonding wires.

48. An assembly as claimed in claim 33 wherein said substrate is a circuit panel.

47
~~49~~. An assembly as claimed in claim ~~33~~ 33 or claim ~~34~~ 34 or claim ~~35~~ 35 or claim ~~36~~ 36 or claim ~~37~~ 37 or claim ~~38~~ 38 or claim ~~39~~ 40 or claim ~~40~~ 42 or claim 43 wherein said dielectric element includes electrically conductive lead portions connected to said

terminals so that electrical connections between at least some contacts on said chips are made through said lead portions.

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50. The assembly as claimed in any of claims 5 through 6 7, wherein the dielectric element is adapted to control the impedance of said lead portions .

49 48

51. The assembly as claimed in claim 50, wherein the dielectric element includes an electrically conductive layer adapted to aid the electrical isolation of the terminals from the chip and to provide better control of impedance in said lead portions.

52. A semiconductor chip assembly, comprising:

a) a first semiconductor chip having a front surface, a rear surface and contacts on said front surface;

b) a second semiconductor chip having a front surface, a rear surface and contacts on said front surface, said rear surface of said second semiconductor chip being juxtaposed with said front surface of said first semiconductor chip;

c) a third semiconductor chip having a front surface, a rear surface and a rear surface, said rear surface of said second semiconductor chip being juxtaposed with said front surface of said second semiconductor chip;

d) a first backing element having electrically conductive first terminals, said first backing element being juxtaposed with said rear surface of said first semiconductor chip so that at least some of said terminals overlie said rear surface of said first semiconductor chip, at least some

A6 Cont'd.

of said contacts on said first and said second semiconductor chips being electrically connected to at least some of said terminals; and

e) a substrate having contact pads thereon, said first terminals being connected to said contact pads of said substrate, said substrate being adapted to connect the assembly with other elements of a circuit, said terminals of said backing element overlying said rear surface of said first semiconductor chip.

51 1
~~53~~. The assembly as claimed in claim 2 wherein said first terminals are movable with respect to said first chip to compensate for differential thermal expansion of said first chip and said substrate.

52 51
~~54~~. The assembly as claimed in claim ~~53~~ wherein said first semiconductor chip and said substrate have different coefficients of thermal expansion.

53 50
~~55~~. The assembly as claimed in claim ~~52~~ wherein said first backing element has electrically conductive lead portions thereon connected to said terminals and wherein said terminals are electrically connected to at least some of said contact on said first and second semiconductor chips through said lead portions.

54 53
~~56~~. The assembly as claimed in claim ~~55~~ further comprising first bonding wires extending between at least some of said contacts of said first semiconductor chip and said lead portions so that said terminals of said first backing element are electrically connected to at least some